REMARKS

The Examiner has objected to Claim 1 due to informalities. Applicant respectfully asserts that the objection is avoided due to amendments made hereinabove to the aforementioned claim.

The Examiner has rejected Claim 2 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully notes that the language of Claim 2 has been amended to claim "further comprising the steps of" in order to avoid the rejection.

The Examiner has rejected Claims 1-12 under 35 U.S.C. 103(a) as being unpatentable over Tarrab (U.S. Patent No. 5,195,093), in view of Yang (U.S. Patent No. 6,701,478). Further, the Examiner has rejected Claim 13 under 35 U.S.C. 103(a) as being unpatentable over Tarrab, in view of Meyer (U.S. Patent No. 5,953,352). Applicant respectfully disagrees with such rejections, especially in view of the amendments made hereinabove to the independent claims.

With respect to independent Claim 5, the Examiner has relied on Figures 4 and 6; Col. 7, lines 4-44; and Col. 10, lines 4-57 from Tarrab to make a prior art showing of applicant's claimed "first multiplexer coupled to said CRC cores for selecting the output of one of said CRC cores based on a number of data blocks output on said data bus" (as currently amended).

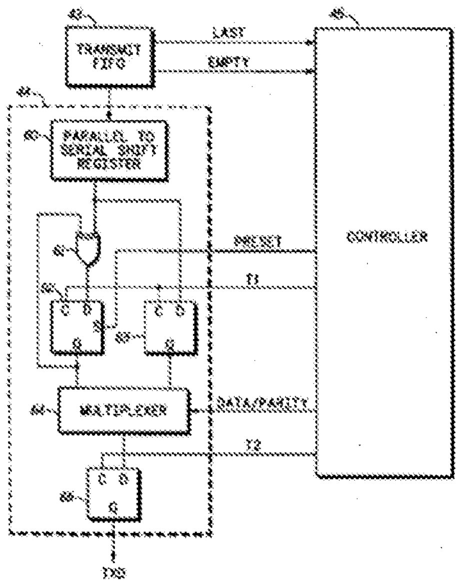


*FIG.6*
(Tarrab, Figure 6)

Applicant respectfully asserts that the figures and excerpts from Tarrab relied upon by the Examiner merely disclose that "the CRC-16 field may be calculated by circuitry located in serial to parallel conversion block 41 and parallel to serial conversion block 44 in the receiver and transmitter, respectively" and that "the CRC-16 field may be calculated by a microcode routine executed by communication processor 26 as data is either read from receive FIFO 40, or provided to transmit FIFO 43" (Col. 7, lines 26-31 – emphasis added). Further, Tarrab discloses that "[p]arallel-to-serial conversion block 44 is shown in greater detail as including a parallel-to-serial shift register 60, an exclusive-OR gate 61, a D-type flip-flop 62, a D-type flip-flop 63, a multiplexer 64, and a D-type flip-flop 65" (Col. 10, lines 26-30 – emphasis added). Additionally, Tarrab discloses that "[m]ultiplexer 64 has a first input terminal coupled to the output terminal of flip-flop 62, a second input terminal coupled to the output terminal of flip-flop 63, and an output terminal" (Col. 10, lines 49-52 – emphasis added).

However, the mere disclosure that the CRC-16 may be calculated by a serial to parallel conversion block 41, a parallel to serial conversion block 44, which includes a multiplexer with inputs from two flip-flops, and a microcode routine executed by communication processor, as in Tarrab, simply fails to even suggest "a first multiplexer

coupled to said CRC cores for selecting the output of one of said CRC cores based on a number of data blocks output on said data bus" (emphasis added), as claimed by applicant. Clearly, a parallel to serial conversion block, which includes a multiplexer with inputs from two flip-flops, as in Tarrab, simply fails to meet "a first multiplexer coupled to said CRC cores for selecting the output of one of said CRC cores" (emphasis added), in the manner as claimed by applicant.

Further, with respect to independent Claim 12, the Examiner has relied on Figure 3 (reproduced below) from the Tarrab reference along with Figure 4 and Col. 6, lines 1-6 (reproduced below) from the Yang reference to make a prior art showing of applicant's claimed "plurality of CRC cores coupled to each of said respective registers, said CRC cores for calculating CRC values for said data blocks stored in each of said registers" (as currently amended). Specifically, the Examiner has admitted that Tarrab does not disclose a plurality of CRC cores, but has argued that the plurality of CRC cores is taught by Yang.

> "Bridging module 400 includes a number of CRC generators 402.sub.1, 402.sub.2, . . . , 402.sub.8 operating in parallel to produce a 4-byte or 32-bit CRC value 404. These parallel CRC generators 402.sub.1, 402.sub.2, . . . , 402.sub.8 are operatively coupled to parallel data bus and generally calculate the CRC value 404 based on a different bit segment of the data bus." (Yang Col. 6, lines 1-6)

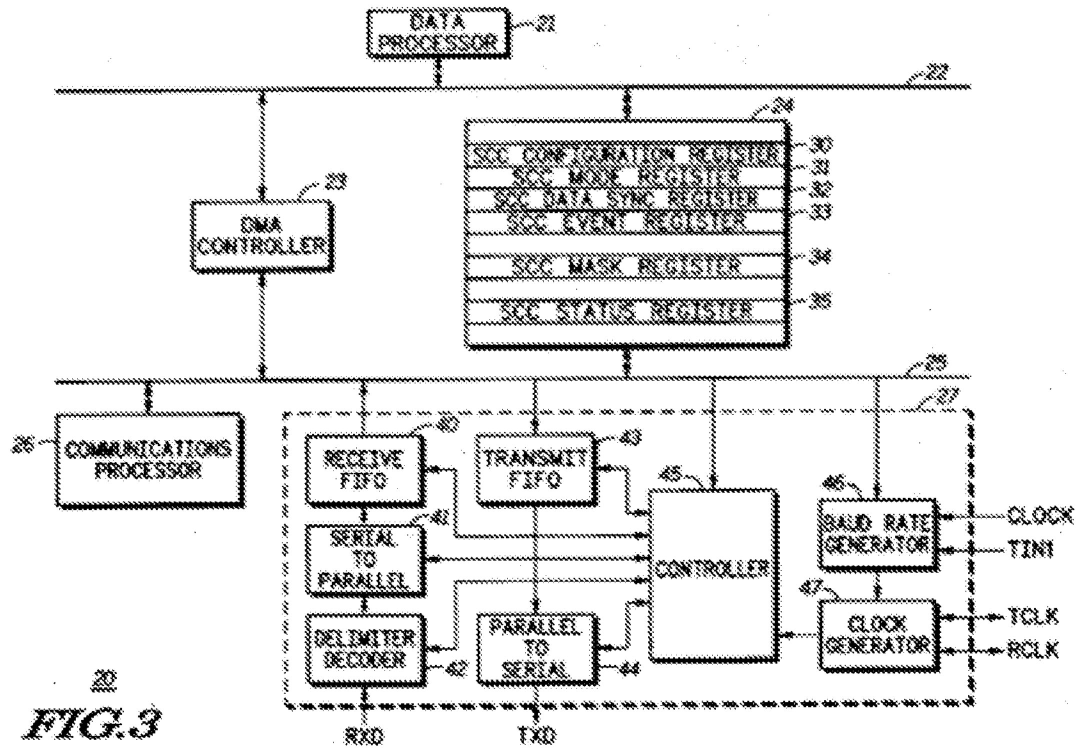


FIG.3

(Tarrab, Figure 3)

Applicant respectfully disagrees and asserts that the description of the figure from Tarrab relied upon by the Examiner merely discloses that the "[d]ata processing system 20 includes a data processor 21, a processor bus 22, a direct memory access (DMA) controller 23, a dual-ported memory 24, a peripheral bus 25, [and] a communication processor 26…" where the "[d]ual-ported memory [24] has several registers…" (Col. 5, lines 40-45 – emphasis added). However, the mere disclosure of a dual-ported memory 24 with several registers connected to processor bus 22 and peripheral bus 25, as in Tarrab, simply fails to even suggest "a plurality of CRC cores coupled to each of said respective registers, said CRC cores for calculating CRC values for said data blocks stored in each of said registers" (emphasis added), as claimed by applicant. Clearly, a dual-ported memory connected to a peripheral bus, as in Tarrab, fails to meet "a plurality of CRC cores coupled to each of said respective registers" (emphasis added), in the manner as claimed by applicant.

Furthermore, with respect to independent Claim 12, the Examiner has relied on Figures 4 and 6; Col. 7, lines 4-44; and Col. 10, lines 4-57 from Tarrab to make a prior

art showing of applicant's claimed "multiplexer for selecting said CRC value calculated by one of said CRC cores, based on which of said plurality of registers contain valid data" (as currently amended).

Applicant respectfully asserts that the figures and excerpts from Tarrab relied upon by the Examiner merely disclose that "the CRC-16 field may be calculated by circuitry located in serial to parallel conversion block 41 and parallel to serial conversion block 44 in the receiver and transmitter, respectively" and that "the CRC-16 field may be calculated by a microcode routine executed by communication processor 26 as data is either read from receive FIFO 40, or provided to transmit FIFO 43" (Col. 7, lines 26-31 – emphasis added). Further, Tarrab discloses that "[p]arallel-to-serial conversion block 44 is shown in greater detail as including a parallel-to-serial shift register 60, an exclusive-OR gate 61, a D-type flip-flop 62, a D-type flip-flop 63, a multiplexer 64, and a D-type flip-flop 65" (Col. 10, lines 26-30 – emphasis added). Additionally, Tarrab discloses that "[m]ultiplexer 64 has a first input terminal coupled to the output terminal of flip-flop 62, a second input terminal coupled to the output terminal of flip-flop 63, and an output terminal" (Col. 10, lines 49-52 – emphasis added).

However, the mere disclosure that the CRC-16 may be calculated by a serial to parallel conversion block 41, a parallel to serial conversion block 44, which includes a multiplexer with inputs from two flip-flops, and a microcode routine executed by communication processor, as in Tarrab, simply fails to even suggest "a multiplexer for selecting said CRC value calculated by one of said CRC cores," let alone "based on which of said plurality of registers contain valid data" (emphasis added), as claimed by applicant. Clearly, a parallel to serial conversion block, which includes a multiplexer with inputs from two flip-flops, as in Tarrab, simply fails to meet "a multiplexer for selecting said CRC value calculated by one of said CRC cores" (emphasis added), in the manner as claimed by applicant.

In addition, with respect to independent Claim 13, the Examiner has relied on Col. 4, lines 13-33 (reproduced below) from the Meyer reference to make a prior art showing

of applicant's claimed "calculating a CRC value in accordance with a predetermined algorithm, utilizing a transport offload engine (TOE)."

> "In an IDE controller having a primary channel and a secondary channel, each channel receives a dataword from one of two mirrored disks. A CRC/checksum calculation is then performed on each dataword and the result is stored in respective accumulation registers for each channel of the IDE controller. Upon receiving the next dataword, <u>each channel performs a CRC/checksum calculation by implementing a predetermined CRC algorithm</u>. In one embodiment, each new dataword is combined with the previously calculated CRC value using XOR gates to implement a specific polynomial function in order to produce a new CRC/checksum value. However, it should be understood that this invention is not limited to any specific CRC or checksum algorithm but may include any one of numerous data integrity algorithms which are well-known in the art. In one embodiment, a dataword is a 16-bit dataword, which is an industry standard. However, datawords having lengths greater than or less than 16-bits may be used in the present invention. As used herein, the term "dataword" refers to any unit of data being a specified number of bits in width, such as, 16-bits or 32-bits." (Col. 4, lines 13-33 - emphasis added)

Applicant respectfully points out that the excerpt from Meyer relied upon by the Examiner merely teaches "an <u>IDE controller</u> having a primary channel and a secondary channel" where "<u>each channel performs a CRC/checksum calculation</u> by implementing a predetermined CRC algorithm" and that "this invention is not limited to any specific CRC or checksum algorithm but may include any one of numerous data integrity algorithms which are well-known in the art" (emphasis added). Further, Meyer discloses "a fast and efficient comparison of <u>cyclic redundancy check (CRC)/checksum values of two mirrored disks</u> in a RAID level 1 system" (Col. 1, lines 7-9) by "providing a hardware implemented compare circuit which simultaneously and concurrently receives data blocks from each of the <u>mirrored disks in a dual channel IDE controller architecture</u>" (Col. 2, lines 48-51 – emphasis added).

However, the mere disclosure of an <u>IDE controller</u> where each channel performs a CRC calculation, as in Meyer, simply fails to even suggest "calculating a CRC value in accordance with a predetermined algorithm, <u>utilizing a transport offload engine (TOE)</u>" (emphasis added), as claimed by applicant. Clearly, calculating CRC for each channel on

an IDE controller, as in Meyer, fails to even suggest "a transport offload engine (TOE)," in the manner as claimed by applicant.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to teach or suggest all of the claim limitations, as noted above. Nevertheless, despite such paramount deficiencies and in the spirit of expediting the prosecution of the present application, applicant has amended the independent claims to substantially include at least a portion of the following claim language in order to further distinguish applicant's claim language from the prior art:

> "wherein data is received using an Internet small computer system interface (iSCSI) protocol;
>
> wherein CRC values are calculated in accordance with a predetermined algorithm that accommodates said data received using the iSCSI protocol, utilizing a transport offload engine (TOE) including a physical data link that provides a physical connection to the Internet, a network stack in communication with said physical data link utilizing a TCP/IP protocol, a storage protocol services processor in communication with said network stack for exchanging data with said network stack, processing requests from a storage application, and encapsulating or decoding packets as requested by said storage application in

accordance with said iSCSI protocol" (see this or similar, but not necessarily identical language in the independent claims).

Applicant respectfully asserts that the Tarrab simply teaches "a method for ensuring CRC error generation by a data communication station experiencing a transmitter exception during a transmission of a frame" (Col. 3, lines 54-57). Further, applicant respectfully asserts that merely Yang teaches that the "[b]ridging module 400 includes a number of… parallel CRC generators… [which] are operatively coupled to parallel data bus and generally calculate the CRC value… based on a different bit segment of the data bus" (Col. 6, lines 1-6). In addition, applicant respectfully points out that the Meyer only teaches an "IDE controller having a primary channel and a secondary channel" where "each channel performs a CRC/checksum calculation by implementing a predetermined CRC algorithm" (Col. 4, lines 13-20).

However, a method for ensuring CRC error generation, as in Tarrab, a bridging module including a number of parallel CRC generators, as in Yang, and an IDE controller where each channel performs a CRC calculation, as in Meyer, all simply fail to disclose a technique "wherein data is received using an Internet small computer system interface (iSCSI) protocol" and "wherein CRC values are calculated in accordance with a predetermined algorithm that accommodates said data received using the iSCSI protocol, utilizing a transport offload engine (TOE) including a physical data link that provides a physical connection to the Internet, a network stack in communication with said physical data link utilizing a TCP/IP protocol, a storage protocol services processor in communication with said network stack for exchanging data with said network stack, processing requests from a storage application, and encapsulating or decoding packets as requested by said storage application in accordance with said iSCSI protocol" (emphasis added), as claimed by applicant.

Thus, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested. All of the independent claims are deemed allowable. Moreover, the

remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP341).

Respectfully submitted,
Zilka-Kotab, PC.

/KEVINZILKA/

Kevin J. Zilka
Registration No. 41,429

P.O. Box 721120
San Jose, CA 95172-1120
408-505-5100